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James E. Smith, Andrew R. Pleszkun

June 1985 **ACM SIGARCH Computer Architecture News , Proceedings of the 12th annual international symposium on Computer architecture ISCA '85**, Volume 13 Issue 3

Publisher: IEEE Computer Society Press, ACM Press

Full text available: pdf(893.17 KB) Additional Information: [full citation](#), [citations](#), [index terms](#)

2 [An executable specification, analyzer and verifier for RMO \(relaxed memory order\)](#)



Seungjoon Park, David L. Dill

July 1995 **Proceedings of the seventh annual ACM symposium on Parallel algorithms and architectures**

Publisher: ACM Press

Full text available: pdf(945.60 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

3 [Data speculation support for a chip multiprocessor](#)



Lance Hammond, Mark Willey, Kunle Olukotun

October 1998 **ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the eighth international conference on Architectural support for programming languages and operating systems ASPLOS-VIII**, Volume 32 , 33 Issue 5 , 11

Publisher: ACM Press

Full text available: pdf(1.75 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Thread-level speculation is a technique that enables parallel execution of sequential applications on a multiprocessor. This paper describes the complete implementation of the support for threadlevel speculation on the Hydra chip multiprocessor (CMP). The support consists of a number of software speculation control handlers and modifications to the shared secondary cache memory system of the CMP This support is evaluated using five representative integer applications. Our results show that the s ...

4 Improving the performance of speculatively parallel applications on the Hydra CMP



Kunle Olukotun, Lance Hammond, Mark Willey

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Publisher: ACM Press

Full text available: [pdf\(1.66 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: chip multiprocessor, data speculation, feedback-driven optimization, multithreading, parallel programming, performance evaluation

5 Cache Memories



Alan Jay Smith

September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3

Publisher: ACM Press

Full text available: [pdf\(4.61 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

6 A dynamic scheduling logic for exploiting multiple functional units in single chip multithreaded architectures



Prasad N. Golla, Eric C. Lin

February 1999 **Proceedings of the 1999 ACM symposium on Applied computing**

Publisher: ACM Press

Full text available: [pdf\(1.19 MB\)](#) Additional Information: [full citation](#), [references](#), [index terms](#)

Keywords: Tomasulo's algorithm, computer architecture, microprocessor, multithreading, threaded architectures

7 Network Protocols



Andrew S. Tanenbaum

December 1981 **ACM Computing Surveys (CSUR)**, Volume 13 Issue 4

Publisher: ACM Press

Full text available: [pdf\(3.37 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

8 Informing memory operations: memory performance feedback mechanisms and their applications



Mark Horowitz, Margaret Martonosi, Todd C. Mowry, Michael D. Smith

May 1998 **ACM Transactions on Computer Systems (TOCS)**, Volume 16 Issue 2

Publisher: ACM Press

Full text available: [pdf\(344.74 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

Memory latency is an important bottleneck in system performance that cannot be adequately solved by hardware alone. Several promising software techniques have been shown to address this problem successfully in specific situations. However, the generality of these software approaches has been limited because current architectures do not provide a fine-grained, low-overhead mechanism for observing and reacting to memory behavior directly. To fill this need, this article proposes a new class ...

Keywords: cache miss notification, memory latency, processor architecture

9 The impact of architectural trends on operating system performance

 M. Rosenblum, E. Bugnion, S. A. Herrod, E. Witchel, A. Gupta
December 1995 **ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles SOSP '95**, Volume 29

Issue 5

Publisher: ACM Press


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10 Informing memory operations: providing memory performance feedback in modern

 processors

Mark Horowitz, Margaret Martonosi, Todd C. Mowry, Michael D. Smith
May 1996 **ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture ISCA '96**, Volume 24 Issue 2

Publisher: ACM Press


Full text available:  [pdf\(1.55 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Memory latency is an important bottleneck in system performance that cannot be adequately solved by hardware alone. Several promising software techniques have been shown to address this problem successfully in specific situations. However, the generality of these software approaches has been limited because current architectures do not provide a fine-grained, low-overhead mechanism for observing and reacting to memory behavior directly. To fill this need, we propose a new class of memory operati ...


11 Some formal language aspects of MARY

Mark Rain
July 1972 **ALGOL Bulletin**, Issue 34


Publisher: Computer History Museum

Full text available:  [pdf\(1.51 MB\)](#) Additional Information: [full citation](#), [index terms](#)


12 A programmable HIPPI interface for a graphics supercomputer

 R. K. Singh, S. G. Tell, S. J. Bharrat, D. Becker, V. L. Chi
December 1993 **Proceedings of the 1993 ACM/IEEE conference on Supercomputing**

Publisher: ACM Press

Full text available:  [pdf\(849.20 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

13 A programmable network interface for a message-based multicomputer

 Raj K. Singh, Stephen G. Tell, Shaun J. Bharrat
July 1994 **ACM SIGCOMM Computer Communication Review**, Volume 24 Issue 3

Publisher: ACM Press

Full text available:  [pdf\(814.91 KB\)](#) Additional Information: [full citation](#), [abstract](#), [index terms](#)

As fiber-optic gigabit networks are being deployed, supercomputer network interfaces are becoming the communication bottleneck. The Network Interface Unit (NIU) is a high-performance network interface for Pixel Planes 5, a custom, message-based multicomputer. The design offers both performance and programmability through a balance of data-handling in hardware an embedded processor. In this paper, we describe

the NIU hardware and firmware architecture. We present results of performance measuremen ...

14 Fixing the Java memory model

 William Pugh

June 1999 **Proceedings of the ACM 1999 conference on Java Grande**

Publisher: ACM Press

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15 A comparative performance evaluation of various state maintenance mechanisms

Michael Butler, Yale Patt


December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**

Publisher: IEEE Computer Society Press

Full text available:  pdf(912.33 KB) Additional Information: [full citation](#), [references](#), [citations](#)




16 Efficient and correct execution of parallel programs that share memory

 Dennis Shasha, Marc Snir

April 1988 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 10 Issue 2


Publisher: ACM Press

Full text available:  pdf(2.35 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)




In this paper we consider an optimization problem that arises in the execution of parallel programs on shared-memory multiple-instruction-stream, multiple-data-stream (MIMD) computers. A program on such machines consists of many sequential program segments, each executed by a single processor. These segments interact as they access shared variables. Access to memory is asynchronous, and memory accesses are not necessarily executed in the order they were issued. An execution is correct if it ...

17 Operating system benchmarking in the wake of Imbench: a case study of the performance of NetBSD on the Intel x86 architecture

 Aaron B. Brown, Margo I. Seltzer

June 1997 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1997 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '97**, Volume 25 Issue 1


Publisher: ACM Press

Full text available:  pdf(1.98 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)



The *Imbench* suite of operating system microbenchmarks provides a set of portable programs for use in cross-platform comparisons. We have augmented the *Imbench* suite to increase its flexibility and precision, and to improve its methodological and statistical operation. This enables the detailed study of interactions between the operating system and the hardware architecture. We describe modifications to *Imbench*, and then use our new benchmark suite, *hbench:OS*, to exami ...

18 A look at several memory management units, TLB-refill mechanisms, and page table organizations

 Bruce L. Jacob, Trevor N. Mudge

October 1998 **ACM SIGOPS Operating Systems Review , ACM SIGPLAN Notices , Proceedings of the eighth international conference on Architectural**



**support for programming languages and operating systems ASPLOS-
VIII**, Volume 32, 33 Issue 5, 11

Publisher: ACM Press

Full text available:  [pdf\(1.90 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Virtual memory is a staple in modern systems, though there is little agreement on how its functionality is to be implemented on either the hardware or software side of the interface. The myriad of design choices and incompatible hardware mechanisms suggests potential performance problems, especially since increasing numbers of systems (even embedded systems) are using memory management. A comparative study of the implementation choices in virtual memory should therefore aid system-level designers ...

19 The SimpleScalar tool set, version 2.0



Doug Burger, Todd M. Austin

June 1997 **ACM SIGARCH Computer Architecture News**, Volume 25 Issue 3

Publisher: ACM Press

Full text available:  [pdf\(985.46 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [citations](#), [index terms](#)

This document describes release 2.0 of the SimpleScalar tool set, a suite of free, publicly available simulation tools that offer both detailed and high-performance simulation of modern microprocessors. The new release offers more tools and capabilities, precompiled binaries, cleaner interfaces, better documentation, easier installation, improved portability, and higher performance. This paper contains a complete description of the tool set, including retrieval and installation instructions, a d ...


20 Memory consistency and event ordering in scalable shared-memory multiprocessors



Kourosh Gharachorloo, Daniel Lenoski, James Laudon, Phillip Gibbons, Anoop Gupta, John Hennessy

May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture ISCA '90**, Volume 18 Issue 3a

Publisher: ACM Press

Full text available:  [pdf\(1.56 MB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Scalable shared-memory multiprocessors distribute memory among the processors and use scalable interconnection networks to provide high bandwidth and low latency communication. In addition, memory accesses are cached, buffered, and pipelined to bridge the gap between the slow shared memory and the fast processors. Unless carefully controlled, such architectural optimizations can cause memory accesses to be executed in an order different from what the programmer expects. The set of allowable ...

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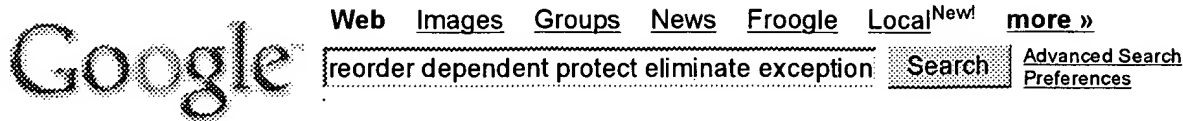
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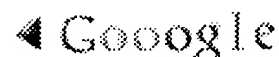
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 Martin, M.M.K.; Sorin, D.J.; Cain, H.W.; Hill, M.D.; Lipasti, M.H.;
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 Kavi, K.M.; Hurson, A.R.;
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 25-28 Oct. 1995 Page(s):182 - 189
 Digital Object Identifier 10.1109/SPDP.1995.530682
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- ☐ **5. High level synthesis of pipelined instruction set processors and back-end**
 Huang, I.-J.; Despain, A.M.;
 Design Automation Conference, 1992. Proceedings., 29th ACM/IEEE
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S23	67	(instruction with reorder\$3) and exception and (categor\$4) and (dependen\$4) and schedul\$3 and violat\$3	USPAT	OR	ON	2002/12/27 14:31
S24	0	(instruction with reorder\$3) and exception and (categor\$4) and (dependen\$4) and morph\$3	USPAT	OR	ON	2002/12/27 14:39
S25	0	(instruction with reorder\$3) and exception and (categor\$4)and morph\$3	USPAT	OR	ON	2002/12/27 14:39
S26	9	(instruction with reorder\$3) and exception and morph\$3	USPAT	OR	ON	2002/12/27 14:39
S27	10	(instruction same re\$order\$3) and exception and (morph\$3)	USPAT	OR	ON	2002/12/27 14:52
S28	3	(instruction same reorder\$3) and exception and (categor\$4 with dependen\$4)	USPAT	OR	ON	2002/12/27 14:57
S29	6	(instruction same re\$order\$3) and exception and (categor\$4 with dependen\$4)	USPAT	OR	ON	2002/12/27 15:00
S30	18	(instruction same re\$order\$3) and exception and (plurality same categor\$4)	USPAT	OR	ON	2002/12/27 15:01
S31	1	("6031992").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/01/20 15:19
S32	1	"5838948".PN.	USPAT	OR	OFF	2003/01/20 15:17
S33	1	"5768567".PN.	USPAT	OR	OFF	2003/01/20 15:18
S34	1	"5721927".PN.	USPAT	OR	OFF	2003/01/20 15:18
S35	1	"5574927".PN.	USPAT	OR	OFF	2003/01/20 15:18
S36	774	(micro\$processor) and (instruct\$3 same re\$order\$3) and (except\$3) and (dependen\$5)	US-PGPUB; USPAT	OR	ON	2003/01/20 15:23

S37	11	(micro\$processor) and (instruct\$3 same re\$order\$3) and (except\$3) and (dependen\$5) and (schedul\$3 with constrain\$3)	US-PGPUB; USPAT	OR	ON	2003/01/20 15:27
S38	12	(micro\$processor) and (instruct\$3 same re\$order\$3) and (except\$3) and (dependen\$5) and (schedul\$3 with constrain\$4)	US-PGPUB; USPAT	OR	ON	2003/01/20 15:28
S39	30	(instruct\$3 same re\$order\$3) and (except\$3) and (dependen\$5) and (schedul\$3 with constrain\$4)	US-PGPUB; USPAT	OR	ON	2003/01/20 15:34
S40	0	(instruct\$3 same re\$order\$3) and (except\$3) and (dependen\$5) and (schedul\$3 with constrain\$4) and morph\$3	US-PGPUB; USPAT	OR	ON	2003/01/20 15:54
S41	9	(instruct\$3 same re\$order\$3) and (except\$3) and (dependen\$5) and morph\$3	US-PGPUB; USPAT	OR	ON	2003/01/20 15:56
S42	2	(instruct\$3 same re\$order\$3) and (except\$3) and (without same dependen\$5) and morph\$3	US-PGPUB; USPAT	OR	ON	2003/01/20 16:02
S43	10	(instruct\$3 same re\$order\$3) and (except\$3) and morph\$3	US-PGPUB; USPAT	OR	ON	2003/01/20 16:02
S44	13	(instruct\$3 same re\$order\$3) and morph\$3	US-PGPUB; USPAT	OR	ON	2003/01/20 16:04
S45	16	(instruct\$3 same translat\$3) and (re\$order\$3) and morph\$3	US-PGPUB; USPAT	OR	ON	2003/01/20 16:05
S46	46	(re\$order\$3) and (morph\$3 same (host or software or code))	US-PGPUB; USPAT	OR	ON	2003/01/20 17:28
S47	1	("6031992").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/01/20 18:46
S48	100	(morph\$3 with (software or host))	US-PGPUB; USPAT	OR	ON	2003/01/20 18:48
S49	17	(morph\$3 with (software or host)) and (re\$order\$3 or re\$arrang\$3)	US-PGPUB; USPAT	OR	ON	2003/01/20 18:49
S50	0	(morph\$3 with (software or host)) and (instruct\$3)	US-PGPUB; USPAT	OR	ON	2003/01/20 18:49
S51	24	(morph\$3 with (software or host)) and (instruct\$3)	US-PGPUB; USPAT	OR	ON	2003/01/20 18:51
S52	77	(morph\$3 same (software or host)) and (instruct\$3)	US-PGPUB; USPAT	OR	ON	2003/01/21 10:21
S53	16	(morph\$3 same (software or host)) and (instruct\$3) and (original with order\$3)	US-PGPUB; USPAT	OR	ON	2003/01/21 11:05
S54	16	(morph\$3 same (software or host)) and (original with order\$3)	US-PGPUB; USPAT	OR	ON	2003/01/21 14:44

S55	3	((("6321272") or ("6282454") or ("6151625"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/01/21 14:44
S56	261	(instruction near4 reorder\$3) and (schedul\$3) and exception and (speed or fast or improv\$3)	USPAT	OR	ON	2003/04/05 16:47
S57	278	(instruction near4 reorder\$3) and (schedul\$3) and exception and (speed or fast or improv\$3)	US-PGPUB; USPAT	OR	ON	2003/04/05 16:47
S58	203	(instruction near4 reorder\$3) and (schedul\$3) and exception and (speed or fast or improv\$3) and "712"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:50
S59	181	(instruction near4 reorder\$3) and (schedul\$3) and exception and (speed or fast or improv\$3) and (dependenc\$3) and "712"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:54
S60	0	(instruction near4 reorder\$3) and (schedul\$3) and exception and (speed or fast or improv\$3) and (probably near3 dependenc\$3) and "712"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:54
S61	0	(instruction near4 reorder\$3) and (schedul\$3) and exception and (speed or fast or improv\$3) and (probabl\$2 near3 dependenc\$3) and "712"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:54
S62	102	(instruction near4 reorder\$3) and (schedul\$3) and exception and (speed or fast or improv\$3) and ((no or probably) with dependenc\$3)	US-PGPUB; USPAT	OR	ON	2003/04/05 16:55
S63	0	(instruction near4 reorder\$3) and (schedul\$3) and exception and (speed or fast or improv\$3) and ((no or probably) with dependenc\$3) and "395"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:55
S64	89	(instruction near4 reorder\$3) and (schedul\$3) and exception and (speed or fast or improv\$3) and ((no or probably) with dependenc\$3) and "712"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:56
S65	2	(schedul\$3 near3 microprocessor).ti.	US-PGPUB; USPAT	OR	ON	2003/04/05 16:57
S66	7	(instruction near4 reorder\$3).ti.	US-PGPUB; USPAT	OR	ON	2003/04/05 17:08
S67	1	"5941980".PN.	USPAT	OR	OFF	2003/04/05 17:04
S68	1	"5933618".PN.	USPAT	OR	OFF	2003/04/05 17:05
S69	1	"5930490".PN.	USPAT	OR	OFF	2003/04/05 17:05

S70	1	"5819057".PN.	USPAT	OR	OFF	2003/04/05 17:05
S71	1	"5778246".PN.	USPAT	OR	OFF	2003/04/05 17:06
S72	1	"5809272".PN.	USPAT	OR	OFF	2003/04/05 17:06
S73	1	"5627983".PN.	USPAT	OR	OFF	2003/04/05 17:06
S74	1	"5613080".PN.	USPAT	OR	OFF	2003/04/05 17:07
S75	1	"5560032".PN.	USPAT	OR	OFF	2003/04/05 17:07
S76	1	"5471593".PN.	USPAT	OR	OFF	2003/04/05 17:07
S77	1	"5560032".PN.	USPAT	OR	OFF	2003/04/05 17:08
S78	55	(instruction near4 (schedul\$3)).ti.	US-PGPUB; USPAT	OR	ON	2003/04/05 17:09
S79	30	((instruction near4 (schedul\$3)).ti.) and re\$order\$3	US-PGPUB; USPAT	OR	ON	2003/04/07 15:02
S80	1	"5655122".PN.	USPAT	OR	OFF	2003/04/05 17:12
S81	1	"5634023".PN.	USPAT	OR	OFF	2003/04/05 17:13
S82	1	"5627981".PN.	USPAT	OR	OFF	2003/04/05 17:15
S83	1	"5421022".PN.	USPAT	OR	OFF	2003/04/05 17:15
S84	1	"5303356".PN.	USPAT	OR	OFF	2003/04/05 17:16
S85	1	"5297281".PN.	USPAT	OR	OFF	2003/04/05 17:16
S86	1	"5269017".PN.	USPAT	OR	OFF	2003/04/05 17:17
S87	1	"5269017".PN.	USPAT	OR	OFF	2003/04/05 17:18
S88	1	"5265213".PN.	USPAT	OR	OFF	2003/04/05 17:18
S89	1	"5201057".PN.	USPAT	OR	OFF	2003/04/05 17:18
S90	1	"5201057".PN.	USPAT	OR	OFF	2003/04/05 17:18
S91	1	"5197138".PN.	USPAT	OR	OFF	2003/04/05 17:18
S92	1	("5421022").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/07 15:21
S93	69	(instruction near5 speculat\$5).ti.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:22
S94	6	((instruction near5 speculat\$5).ti.) and categor\$3	US-PGPUB; USPAT	OR	ON	2003/04/07 15:55
S95	11	((instruction near5 speculat\$5).ti.) and probabl\$2	US-PGPUB; USPAT	OR	ON	2003/04/07 15:55
S96	800	adler.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:26
S97	0	michael-adler.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:24
S98	4	adler-michael.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:24
S99	0	((((instruction near5 speculat\$5).ti.) and probabl\$2) and "395"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:27

S10 0	0	((instruction near5 speculat\$5).ti.) and probabl\$2) and "709"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:26
S10 1	0	adler.in. and "395"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:27
S10 2	7	adler.in. and "709"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:27
S10 3	51	mckeen.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:29
S10 4	21	lowney.in.	US-PGPUB; USPAT	OR	ON	2003/04/07 16:50
S10 5	1	("6377997").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/08 09:52
S10 6	1	("5421022").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/08 10:30
S10 7	1	("5627981").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/08 11:14
S10 8	1	("5901308").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/08 14:11
S10 9	1	("5526499").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/09 10:56
S11 0	8	((("5421022") or ("5526499") or ("5901308") or ("5625837") or ("6065115") or ("6185668") or ("5627981") or ("5269017"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/04/09 10:57
S11 1	1	("5875340").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/13 11:15
S11 2	5	((("5467473") or ("5241633") or ("5202975") or ("5185871") or ("5590295"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/13 14:37
S11 3	1	"5261071".PN.	USPAT	OR	OFF	2003/11/13 12:37
S11 4	1	"5253349".PN.	USPAT	OR	OFF	2003/11/13 12:41
S11 5	1	"5241633".PN.	USPAT	OR	OFF	2003/11/13 12:43
S11 6	1	"5202975".PN.	USPAT	OR	OFF	2003/11/13 12:44
S11 7	1	"5185871".PN.	USPAT	OR	OFF	2003/11/13 12:44
S11 8	1	"5136697".PN.	USPAT	OR	OFF	2003/11/13 12:44

S11 9	1	"5133077".PN.	USPAT	OR	OFF	2003/11/13 12:45
S12 0	1	"5131086".PN.	USPAT	OR	OFF	2003/11/13 12:45
S12 1	1	"5051940".PN.	USPAT	OR	OFF	2003/11/13 12:46
S12 2	1	"4991090".PN.	USPAT	OR	OFF	2003/11/13 12:46
S12 3	1	"4965716".PN.	USPAT	OR	OFF	2003/11/13 12:46
S12 4	1	"4905200".PN.	USPAT	OR	OFF	2003/11/13 12:47
S12 5	1	"4831517".PN.	USPAT	OR	OFF	2003/11/13 12:47
S12 6	1	"4831517".PN.	USPAT	OR	OFF	2003/11/13 12:47
S12 7	1	"4827405".PN.	USPAT	OR	OFF	2003/11/13 12:47
S12 8	1	"5016208".PN.	USPAT	OR	OFF	2003/11/13 12:48
S12 9	1	"4977534".PN.	USPAT	OR	OFF	2003/11/13 12:49
S13 0	1	"4926476".PN.	USPAT	OR	OFF	2003/11/13 12:49
S13 1	1	"4926374".PN.	USPAT	OR	OFF	2003/11/13 12:49
S13 2	1	"4916696".PN.	USPAT	OR	OFF	2003/11/13 12:49
S13 3	1	("6594701").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/13 14:40
S13 4	1	("6347337").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/13 15:35
S13 5	1	("5958019").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/14 14:47
S13 6	0	("(outadj2order\$3)and(eliminat\$3 near3instruction)").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2003/11/14 14:48
S13 7	333	(out adj2 order\$3) and (eliminat\$3 near3 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 15:11
S13 8	196	((out adj2 order\$3) and (eliminat\$3 near3 instruction)) and (store adj3 instruction) and (load adj3 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 15:10

S13 9	5	((out adj2 order\$3) and (eliminat\$3 near3 instruction)) and (store adj3 instruction) and (load adj3 instruction) and (protect\$3 adj3 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 14:52
S14 0	5	((out adj2 order\$3) and (eliminat\$3 near3 instruction)) and (store adj3 instruction) and (load adj3 instruction) and (protect\$3 adj3 register)	US-PGPUB; USPAT	OR	ON	2003/11/14 14:52
S14 1	8	((out adj2 order\$3) and (eliminat\$3 near3 instruction)) and (second near3 (store adj3 instruction)) and (second near3 (load adj3 instruction))	US-PGPUB; USPAT	OR	ON	2003/11/14 14:58
S14 2	184	(out adj2 order\$3) and (eliminat\$3 adj3 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 15:11
S14 3	102	((out adj2 order\$3) and (eliminat\$3 adj3 instruction)) and (load adj2 instruction) and (store adj2 instruction)	US-PGPUB; USPAT	OR	ON	2003/11/14 15:11
S14 4	28	((out adj2 order\$3) and (eliminat\$3 adj3 instruction)) and (load adj2 instruction) and (store adj2 instruction) and (mask)	US-PGPUB; USPAT	OR	ON	2004/05/11 16:52
S14 5	2	((out adj2 order\$3) and (eliminat\$3 adj3 instruction)) and (load adj2 instruction) and (store adj2 instruction) and (mask) and protect	US-PGPUB; USPAT	OR	ON	2003/11/14 15:12
S14 6	0	(wireless adj3 authenticat\$3) and gsm and "802.11" and umts and (mobile adj3 ip)	USPAT	OR	ON	2004/05/10 19:59
S14 7	0	(wireless adj3 authenticat\$3) and gsm and "802.11" and umts	USPAT	OR	ON	2004/05/10 19:59
S14 8	1	(wireless adj3 authenticat\$3) and gsm and umts	USPAT	OR	ON	2004/05/10 20:00
S14 9	5	(wireless near3 authenticat\$3) and gsm and umts	USPAT	OR	ON	2004/05/10 20:02
S15 0	-2	(wireless near3 authenticat\$3) and gsm and "802.11"	USPAT	OR	ON	2004/05/10 20:03
S15 1	5	(wireless near3 authenticat\$3) and (mobile adj3 ip)	USPAT	OR	ON	2004/05/10 20:03
S15 2	6	((("6629207") or ("5751996") or ("5553256") or ("5519841") or ("6549930") or ("6453278"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 16:29
S15 3	1	("5754812").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 16:12

S15 4	1	("5799165").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 16:30
S15 5	1	("5884059").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 16:30
S15 6	1	"5517615".PN.	USPAT	OR	OFF	2004/05/11 16:50
S15 7	1	"5463767".PN.	USPAT	OR	OFF	2004/05/11 16:51
S15 8	1	"5239646".PN.	USPAT	OR	OFF	2004/05/11 16:51
S15 9	1	"5623628".PN.	USPAT	OR	OFF	2004/05/11 16:51
S16 0	1	"5317720".PN.	USPAT	OR	OFF	2004/05/11 16:51
S16 1	1	"5247648".PN.	USPAT	OR	OFF	2004/05/11 16:52
S16 2	240	((out same order\$3)).ti.	US-PGPUB; USPAT	OR	ON	2004/05/11 16:53
S16 3	123	((out same order\$3)).ti.) and (stor\$3 adj3 instruction) and (load\$3 adj3 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:06
S16 4	14	((out same order\$3)).ti.) and (stor\$3 adj3 instruction) and (load\$3 adj3 instruction) and (eliminat\$3 adj4 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:02
S16 5	1	("5,737,636").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/11 17:02
S16 6	3	((out same order\$3)).ti.) and (stor\$3 adj3 instruction) and (load\$3 adj3 instruction) and (protect\$3 near3 register)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:49
S16 7	72	((out same order\$3)).ti.) and (stor\$3 adj3 instruction) and (load\$3 adj3 instruction) and (speculat\$3)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:16
S16 8	5	((out same order\$3)).ti.) and (stor\$3 adj3 instruction) and (load\$3 adj3 instruction) and (speculat\$3) and (eliminat\$3 near3 (load\$3 or stor\$3))	US-PGPUB; USPAT	OR	ON	2004/05/11 17:19
S16 9	6	((out same order\$3)).ti.) and (stor\$3 adj3 instruction) and (load\$3 adj3 instruction) and (speculat\$3) and (address\$3 near3 conflict\$3)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:19

S17 0	110	(first adj4 instruction) and (second adj3 instruction) and (third adj3 instruction) and (address\$3 near3 conflict\$3)	US-PGPUB; USPAT	OR	ON	2004/05/11 17:50
S17 1	18	(first adj4 instruction) and (second adj3 instruction) and (third adj3 instruction) and (address\$3 near3 conflict\$3) and (out\$3 order)	US-PGPUB; USPAT	OR	ON	2004/05/11 18:57
S17 2	15	(first adj4 instruction) and (second adj3 instruction) and (third adj3 instruction) and (address\$3 near3 conflict\$3) and (re\$3 order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:03
S17 3	1	"5517628".PN.	USPAT	OR	OFF	2004/05/11 19:00
S17 4	1	"5509130".PN.	USPAT	OR	OFF	2004/05/11 19:00
S17 5	1	"5371684".PN.	USPAT	OR	OFF	2004/05/11 19:00
S17 6	4	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (address\$3 near3 conflict\$3) and (eliminat\$3 adj3 instruction) and (re\$3 order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:09
S17 7	5	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (address\$3 near3 conflict\$3) and (eliminat\$3 adj3 instruction) and (out\$3 order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:11
S17 8	9	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (address\$3 near3 portion) and (eliminat\$3 adj3 instruction) and (out\$3 order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:13
S17 9	7	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (eliminat\$3 adj3 instruction) and (out\$3 order)	US-PGPUB; USPAT	OR	ON	2004/05/11 19:15
S18 0	7	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (conflict\$3 near3 instruction) and (out\$3 order)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:13
S18 1	1	"5257354".PN.	USPAT	OR	OFF	2004/05/11 19:27
S18 2	50	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (reduc\$4\$3 near3 instruction) and (out\$3 order)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:25

S18 3	1	("5519841").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/12 14:19
S18 4	1	("5926832").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/12 14:19
S18 5	29	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (reduc\$4\$3 near3 instruction) and (out\$ \$order) and (shadow\$3 near3 register)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:25
S18 6	0	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (reduc\$4\$3 near3 instruction) and (out\$ \$order) and (shadow\$3 near3 register) and redundan\$3	US-PGPUB; USPAT	OR	ON	2004/05/12 14:26
S18 7	0	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (reduc\$4\$3 near3 instruction) and (out\$ \$order) and (shadow\$3 near3 register) and redundan\$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:26
S18 8	1	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (reduc\$4\$3 near3 instruction) and (out\$ \$order) and redundan\$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:28
S18 9	1	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (alias near3 memory) and (out\$ \$order) and redundan\$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:29
S19 0	1	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (alias\$3 near3 memory) and (out\$ \$order) and redundan\$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:29
S19 1	0	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (persistent near3 register) and (out\$ \$order) and redundan\$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:29
S19 2	0	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (instruction near3 interven\$3) and (shadow near3 register) and (out\$ \$order) and redundan\$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:29

S19 3	10	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (shadow near3 register) and (out\$3 order) and redundan\$6	US-PGPUB; USPAT	OR	ON	2004/05/12 14:42
S19 4	4	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (access\$3 near3 redundan\$6)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:45
S19 5	6	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (eliminat\$3 near3 (memory adj4 access\$3))	US-PGPUB; USPAT	OR	ON	2004/05/12 14:48
S19 6	111	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (alias\$3 near3 address)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:49
S19 7	17	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (alias\$3 near3 operation)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:54
S19 8	33	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and ((long or short) near4 term) and flag	US-PGPUB; USPAT	OR	ON	2004/05/12 14:54
S19 9	0	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and ((long or short) near4 term) and flag and (alias and shadow)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:55
S20 0	10	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and ((long or short) near4 term) and flag and (shadow)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:56
S20 1	73	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (shadow near3 register)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:56
S20 2	69	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (shadow near3 register) and (long or short)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:57
S20 3	23	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (shadow near3 register) and (commit)	US-PGPUB; USPAT	OR	ON	2004/05/12 14:57
S20 4	0	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (shadow near3 register) and (commit) and rollback	US-PGPUB; USPAT	OR	ON	2004/05/12 14:58

S20 5	23	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (shadow near3 register) and (commit)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:20
S20 6	0	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (shadow near3 register) and (load near3 protect\$3)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:20
S20 7	44	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (load near3 protect\$3)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:51
S20 8	1	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and (load near3 protect\$3) and (commit or rollback)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:21
S20 9	270	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and ((eliminat\$3 or skip\$4) near3 (instruction or operation))	US-PGPUB; USPAT	OR	ON	2004/05/12 15:52
S21 0	4	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and ((eliminat\$3 or skip\$4) near3 (instruction or operation)) and (protect\$3 near3 register)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:55
S21 1	190	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and ((eliminat\$3 or skip\$4) near3 (instruction or operation)) and ("712"/\$.ccls.)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:55
S21 2	81	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and ((eliminat\$3 or skip\$4) near3 (instruction or operation)) and protect\$3 and ("712"/\$.ccls.)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:56
S21 3	5	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$3 order) and ((eliminat\$3 or skip\$4) near3 (instruction or operation)) and protect\$3 and ("712"/\$.ccls.) and (address near3 range)	US-PGPUB; USPAT	OR	ON	2004/05/12 15:59

S21 4	169	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$\$order) and ((eliminat\$3 or skip\$4) near3 (instruction or operation)) and sequenc\$3 and ("712"/\$.ccls.)	US-PGPUB; USPAT	OR	ON	2004/05/12 16:00
S21 5	144	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$\$order) and ((eliminat\$3 or skip\$4) near3 (instruction or operation)) and (sequenc\$3 near3 instruction) and ("712"/\$.ccls.)	US-PGPUB; USPAT	OR	ON	2004/05/12 17:19
S21 6	42	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$\$order) and ((eliminat\$3 or skip\$4) near3 (instruction or operation)) and (sequenc\$3 near3 instruction) and ("712"/\$.ccls.) and ((load\$3 or stor\$3) near3 protect\$3)	US-PGPUB; USPAT	OR	ON	2004/05/12 16:58
S21 7	1	("5519841").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/12 17:13
S21 8	1	("5931957").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2004/05/12 17:14
S21 9	41	(load\$3 adj4 instruction) and (stor\$3 adj3 instruction) and (out\$\$order) and ((eliminat\$3 or skip\$4) near3 (instruction or operation)) and (sequenc\$3 near3 instruction) and ("712"/\$.ccls.) and redundan\$6	US-PGPUB; USPAT	OR	ON	2004/05/12 18:20
S22 0	426	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out\$\$order)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:21
S22 1	5	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out\$\$order) and re\$\$order and (protect\$3 near3 address)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:23
S22 2	25	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out\$\$order) and re\$\$order and (protect\$3 near3 load)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:24

S22 3	170	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out\$\$order) and re\$\$order and "712"/\$.ccls.	US-PGPUB; USPAT	OR	ON	2004/05/12 18:25
S22 4	68	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out\$\$order) and re\$\$order and "712"/\$.ccls. and mask\$3	US-PGPUB; USPAT	OR	ON	2004/05/12 18:45
S22 5	85	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out\$\$order) and re\$\$order and ((eliminat\$3 or skip\$4) near3 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:46
S22 6	57	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out\$\$order) and re\$\$order and ((eliminat\$3) near3 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/12 18:58
S22 7	36	(first adj3 (operation or instruction)) and (second adj3 (operation or instruction)) and (third adj3 (operation or instruction)) and (out\$\$order) and re\$\$order and ((skip\$4) near3 instruction)	US-PGPUB; USPAT	OR	ON	2004/05/13 10:29
S22 8	1	((load or store) adj3 protect) near3 instruction	US-PGPUB; USPAT	OR	ON	2004/05/13 10:30
S22 9	10	((load or store) adj3 protect) near3 operation	US-PGPUB; USPAT	OR	ON	2004/05/13 13:20
S23 0	1	("6513110").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/02 10:36
S23 1	2	((("5519841") or ("5920710"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/02 11:07
S23 2	3	((("6011908") or ("5832205") or ("5918005"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/02 11:25
S23 3	1	"5689712".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:21
S23 4	1	"5625835".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:21

S23 5	1	"5542075".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:22
S23 6	1	"5421022".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:22
S23 7	1	"5420990".PN.	USPAT; USOCR	OR	ON	2005/05/02 11:22
S23 8	279	(out same order\$3).ti.	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/02 11:25
S23 9	85	(out same order\$3).ti. and re\$\$order\$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/02 11:26
S24 0	52	(out same order\$3).ti. and re\$\$order\$3 and stor\$3 and load\$3 and except\$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/02 11:26
S24 1	781	(instruct\$3 near4 schedul\$3) and dependen\$3 and (out near4 order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 18:38
S24 2	456	(instruct\$3 near4 schedul\$3) and dependen\$3 and (out near4 order\$3) and stor\$3 and load\$3 and eliminat\$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:38
S24 3	97	(instruct\$3 near4 schedul\$3) and dependen\$3 and (out near4 order\$3) and stor\$3 and load\$3 and (eliminat\$3 near4 instruct\$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 18:39
S24 4	68	(instruct\$3 near4 schedul\$3) and dependen\$3 and (out near4 order\$3) and stor\$3 and load\$3 and (eliminat\$3 near4 instruct\$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 18:39
S24 5	18	(instruct\$3 near4 schedul\$3) and (address\$3 near4 dependen\$3) and (out near4 order\$3) and stor\$3 and load\$3 and (eliminat\$3 near4 instruct\$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 18:46
S24 6	1	("5754812").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/03 18:45
S24 7	52	(address\$3 near4 dependen\$3) and (out near4 order\$3) and (stor\$3 near4 load\$3) and (eliminat\$3 near4 instruct\$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 18:46
S24 8	43	(address\$3 near4 dependen\$3) and (out near4 order\$3) and (stor\$3 near4 load\$3) and (eliminat\$3 near4 instruct\$3) and (@ad<"19990614") and schedul\$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:51

S24 9	45	(address\$3 near4 dependen\$3) and (re\$3order\$3) and (stor\$3 near4 load\$3) and (eliminat\$3 near4 instruct\$3) and (@ad<"19990614") and schedul\$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:55
S25 0	42	(address\$3 near4 dependen\$3) and (re\$3order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614") and schedul\$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:57
S25 1	37	(address\$3 near4 dependen\$3) and (out near4 order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614") and schedul\$3	US-PGPUB; USPAT	OR	ON	2005/05/03 18:59
S25 2	51	(address\$3 near4 dependen\$3) and (out near4 order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:04
S25 3	1001	(out near4 order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:04
S25 4	970	(re\$3order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:05
S25 5	29	(re\$3order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614") and (schedul\$3 near4 instruct\$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:08
S25 6	3	(re\$3order\$3) and (eliminat\$3 near4 sequenc\$3) and (stor\$3 and load\$3) and (@ad<"19990614") and (schedul\$3 near4 instruct\$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:11
S25 7	0	(our near4 order\$3) and (eliminat\$3 near4 sequenc\$3) and (stor\$3 and load\$3) and (@ad<"19990614") and (schedul\$3 near4 instruct\$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:11
S25 8	1	(our near4 order\$3) and (eliminat\$3 near4 sequenc\$3) and (stor\$3 and load\$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:12
S25 9	1357	(eliminat\$3 near4 sequenc\$3) and (stor\$3 and load\$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:12
S26 0	5660	(eliminat\$3 near4 operation) and (stor\$3 and load\$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:13

S26 1	645	(out near4 order\$3) and (eliminat\$3 near4 operation) and (stor\$3 and load\$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:13
S26 2	144	(out near4 order\$3) and (eliminat\$3 near4 operation) and (stor\$3 and load\$3) and (@ad<"19990614") and (re\$order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:13
S26 3	22	(out near4 order\$3) and (eliminat\$3 near4 operation) and (stor\$3 and load\$3) and (@ad<"19990614") and (re\$order\$3) and (schedul\$3 near4 execut\$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:14
S26 4	248	(out near4 order\$3) and (eliminat\$3 near4 operation) and (stor\$3 near5 load\$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:14
S26 5	87	(out near4 order\$3) and (eliminat\$3 near4 operation) and (stor\$3 near5 load\$3) and (@ad<"19990614") and re\$order\$3	US-PGPUB; USPAT	OR	ON	2005/05/03 19:14
S26 6	67	(out near4 order\$3) and (eliminat\$3 near4 operation) and (stor\$3 near5 load\$3) and (@ad<"19990614") and re\$order\$3 and schedul\$3	US-PGPUB; USPAT	OR	ON	2005/05/03 19:23
S26 7	131	(address\$3 near4 dependen\$3) and (eliminat\$3 near4 (instruct\$3 or operation)) and (stor\$3 near5 load\$3) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/03 19:23
S26 8	68	(address\$3 near4 dependen\$3) and (eliminat\$3 near4 (instruct\$3 or operation)) and (stor\$3 near5 load\$3) and (@ad<"19990614") and (re\$order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/03 19:28
S26 9	57	(address\$3 near4 dependen\$3) and (eliminat\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614") and (re\$order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/04 09:45
S27 0	36	(address\$3 near4 dependen\$3) and (eliminat\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614") and (redundant)	US-PGPUB; USPAT	OR	ON	2005/05/04 09:47
S27 1	12	(redundant near4 instruct\$3) and (eliminat\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/04 10:15
S27 2	1	"6029005".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:02

S27 3	1	"5797013".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:02
S27 4	1	"5787285".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:03
S27 5	1	"5751983".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:03
S27 6	1	"5704053".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:11
S27 7	1	"5555412".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:11
S27 8	1	"5537620".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:12
S27 9	1	"5526499".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:12
S28 0	1	"5293631".PN.	USPAT; USOCR	OR	ON	2005/05/04 10:14
S28 1	104	(eliminat\$3 near4 instruct\$3) and (dependen\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614")	US-PGPUB; USPAT	OR	ON	2005/05/04 10:15
S28 2	21	(eliminat\$3 near4 instruct\$3) and (dependen\$3 near4 (stor\$3 or load\$3)) and (@ad<"19990614") and re\$execut\$3	US-PGPUB; USPAT	OR	ON	2005/05/04 14:29
S28 3	1	("5519841").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/04 14:29
S28 4	118	(protect\$3 near4 registry)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:47
S28 5	7	(protect\$3 near4 registry) and (re\$\$order\$3 or out\$\$order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:51
S28 6	197	(protect\$3 near4 register) and (re\$\$order\$3 or out\$\$order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:52
S28 7	132	(protect\$3 adj4 register) and (re\$\$order\$3 or out\$\$order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:53
S28 8	111	(protect\$3 adj4 register) and (re\$\$order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:53
S28 9	111	(protect\$3 adj4 register) and (re\$\$order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:53
S29 0	4	(protect\$3 adj4 register) and (re\$\$order\$3 near4 instruct\$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:57
S29 1	2	(protect\$3 near4 (load or store) near4 register) and (re\$\$order\$3 near4 instruct\$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:58
S29 2	191	(protect\$3 near4 (load or store) near4 register)	US-PGPUB; USPAT	OR	ON	2005/05/13 15:58

S29 3	12	(protect\$3 near4 (load or store) near4 register) and (re\$order\$3)	US-PGPUB; USPAT	OR	ON	2005/05/13 18:34
S29 4	0	("(segmentnear4identifier)andvirtu al").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/13 18:35
S29 5	576	(segment near4 identifier) and virtual	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/13 18:35
S29 6	61	(segment near4 identifier) and (virtual near4 circuit)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/13 18:37
S29 7	30	(segment near4 identifier) and (virtual near4 circuit) and (configur\$7 near4 system)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/13 19:12
S29 8	1	("6513110").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 12:08
S29 9	319	(out near4 order\$3) and (re\$order\$3) and (eliminat\$3 near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:09
S30 0	258	(out near4 order\$3) and (re\$order\$3) and (eliminat\$3 near4 instruction) and (stor\$3 near4 load\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:09
S30 1	309	(out near4 order\$3) and (re\$order\$3) and (eliminat\$3 near4 instruction) and ((stor\$3 or load\$3) near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:10
S30 2	69	(out near4 order\$3) and (re\$order\$3) and (eliminat\$3 near4 instruction) and ((stor\$3 or load\$3) near4 instruction) and (address\$3 near4 dependen\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:23
S30 3	111	(out near4 order\$3) and (re\$order\$3) and (reduc\$3 near4 instruction) and ((stor\$3 or load\$3) near4 instruction) and (address\$3 near4 dependen\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:23
S30 4	86	(out near4 order\$3) and (re\$order\$3) and (reduc\$3 near4 instruction) and ((stor\$3 or load\$3) near4 instruction) and (address\$3 near4 dependen\$3) and eliminat\$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:24
S30 5	2	(out near4 order\$3) and (re\$order\$3) and (reduc\$3 near4 instruction) and (eliminat\$3 near4 (stor\$3 or load\$3) near4 instruction) and (address\$3 near4 dependen\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:25

S30 6	4	(out near4 order\$3) and (re\$order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3) near4 instruction) and (address\$3 near4 dependen\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:26
S30 7	5	(re\$order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3) near4 instruction) and (address\$3 near4 dependen\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:28
S30 8	57	(re\$order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3) near4 instruction) and (dependen\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:29
S30 9	48	(re\$order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3) near4 instruction) and (dependen\$3) and exception	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:41
S31 0	26	(re\$order\$3) and (eliminat\$3 near4 (stor\$3 or load\$3) near4 instruction) and (dependen\$3) and exception and protect\$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:30
S31 1	19	(eliminat\$3 near4 (stor\$3 or load\$3) near4 instruction) and (check\$3 near4 dependen\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:45
S31 2	124	(eliminat\$3 near4 instruction) and (check\$3 near4 dependen\$3) and (load\$3 near4 stor\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 12:46
S31 3	102	(eliminat\$3 near4 instruction) and (check\$3 near4 dependen\$3) and ((load\$3 near4 stor\$3) near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 13:13
S31 4	6	(eliminat\$3 near4 instruction) and (check\$3 near4 dependen\$3) and ((load\$3 near4 stor\$3) near4 protect\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 13:23
S31 5	1	(eliminat\$3 near4 instruction)and ((load\$3 near4 stor\$3) near4 protect\$3 near4 register\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 13:24
S31 6	12	(eliminat\$3 near4 instruction)and ((load\$3 or stor\$3) near4 protect\$3 near4 register\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 13:28
S31 7	29	(eliminat\$3 near4 instruction)and ((load\$3 or stor\$3) near4 protect\$3 near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:00
S31 8	301	(eliminat\$3 near4 load\$3 near4 stor\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:00
S31 9	93	(eliminat\$3 near4 load\$3 near4 stor\$3) and re\$order\$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:01

S32 0	82	(eliminat\$3 near4 load\$3 near4 stor\$3) and re\$ \$order\$3 and exception	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:10
S32 1	3	(eliminat\$3 near4 load\$3 near4 stor\$3) and re\$ \$order\$3 and exception and interferenc\$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:02
S32 2	24	(eliminat\$3 near4 load\$3 near4 stor\$3) and re\$ \$order\$3 and exception and re\$ \$execut\$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:13
S32 3	221	((load\$3 or stor\$3) near4 dependen\$3) and (eliminat\$3 near4 instruction)	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:13
S32 4	31	((load\$3 or stor\$3) near4 dependen\$3) and (eliminat\$3 near4 instruction) and exception and re\$ \$execut\$3	US-PGPUB; USPAT; USOCR	OR	ON	2005/05/25 15:28
S32 5	1	("5901308").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 15:28
S32 6	1	("5918005").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 19:33
S32 7	1	("6076166").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 19:33
S32 8	1	("6854370").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 19:34
S32 9	4	((("6845370") or ("5701451") or ("5727174") or ("5740362"))).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/25 19:34